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EXAMINER	
GRAHAM, KRETELIA	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/986,290	LANDFIELD ET AL.	
	Examiner	Art Unit	
	KRETELIA GRAHAM	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15,18 and 19* is/are pending in the application.

4a) Of the above claim(s) *5,6,9-11,18 and 19* is/are withdrawn from consideration.

5)☒ Claim(s) *4* is/are allowed.

6)☒ Claim(s) *1-3,7,8,12,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 10/22/08, with respect to the objection to the claims have been fully considered and are persuasive. The objection has been withdrawn.

2. Applicant's arguments with respect to claim 12 have been considered but are moot in view of the new ground(s) of rejection in view of newly discovered prior art to Pomet et al. (US 5,963,505).

3. Applicant's arguments with respect to claims 1, 2, 7, and 13 have been fully considered but they are not persuasive.

Pertaining to claims 1 and 2, Applicant's arguments that Oda (US 5,644,387) does not teach a matrix connecting parallel and perpendicular arrays (see page 10 of the Remarks) are not persuasive. It is noted that the features upon which applicant relies (i.e., parallel and perpendicular arrays) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants further argue that Oda also fails to disclose sequentially connected arrays, means for applying temporally sequential information to the array, and means for successively latching and disabling each memory storage unit (see page 9 of the

Remarks). These arguments are also not persuasive. As shown in Fig. 1 of Oda, registers 13, 17, 19 and 23, 25, and 27 are connected in sequence. Data is transmitted sequentially from one register to the next through bus lines 14 and 16, and each registers is disabled/enabled according to signals L1EN-L6EN (also see Fig. 6).

For these reasons, the Examiner believes that all claimed subject matter is taught by Figs.1 and 6 of Oda. Therefore, the rejection of claims 1 and 2 is maintained.

Pertaining to claims 7 and 13, Applicant's arguments that Oda fails to disclose storing temporally sequential information in an array and retrieving and reading the information in the same order as it was initially restored (see page 11 of the Remarks) are not persuasive. As shown at Table I in column 8, when signal RSTL is even the information is read out in the same order as which is was latched (also see column 8, lines 41-47), as required by claims 7 and 13. For this reason, the Examiner believes that all claimed subject matter is taught by Oda. Therefore, the rejections of claims 7 and 13 are maintained.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 3 rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the US patent to Oda et al. (5,644,387).

Pertaining to claim 1, **Fig. 1** is directed towards: A memory matrix device **11** for storing temporally sequential information **12** in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial sequential access memory, a random access memory or a dynamic random access memory **Note: Data register 11 of Fig. 1 does not use memory addresses to address data and is neither a DRAM, serial sequential access memory, or a RAM**, comprising: sequentially-connected arrays of fixed memory storage units **17, 19, 21, 23, 25, 27**; means for applying **14,16** the temporally sequential information to the arrays of fixed memory storage units **see column 2, line 63 – column 3, line 2**; and means for successively latching and disabling **29, L1EN, L2EN, L3EN, L4EN, L5EN, L6EN** each successive fixed memory storage unit in a sequentially-connected array of said units each array becoming enabled and then un-enabled in temporal sequence , thereby directing the next temporal bit of information to the next memory storage unit in said sequentially connected array, and wherein, the input to the sequentially-connected array of fixed memory storage units is disabled upon completion of storage of a temporally sequential event to prevent overwriting **Note: Data D0-D8 is transferred to latches 13, 17, 19, 21, 23, 25, 27 in response a respective latch enable signal L1EN, L2EN,**

L3EN, L4EN, L5EN, L6EN. See Fig. 6 where each latch accepts data at the rising edge of the respective latch enable signal and does not accept a new data bit when a latch enable signal is logic low (disabled). The claim limitation "to prevent overwriting" is met by the prior art (Oda), since Oda discloses in Fig. 6 that data is only transferred to a latch when its corresponding latch enable signal is enabled or "logic high". It is obvious that overwriting is prevented since each latch is enabled and receives data only during certain time periods (logic high latch enable signals) and the data is not continuously being stored in the latch. See MPEP 2183 (D).

Pertaining to claim 3, **Fig.1** is directed towards: wherein the array of fixed memory storage units includes semiconductor memory devices **Note: See Fig. 1 where latches 17, 19, 21, 23, 25, and 27 are registers used to store data of a memory**.

6. Claims 2, 7, 8, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Oda.

Pertaining to claim 2, **Fig. 1** is directed towards: A memory matrix device **11** for storing temporally sequential information **12** in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial sequential access memory, a random access memory or a dynamic random access memory **Note: Data register 11 of Fig. 1 does not use memory addresses to address data and is neither a DRAM, serial sequential access memory, or a RAM**, comprising: sequentially-connected arrays of fixed memory storage units **17, 19, 21, 23,**

25, 27; means for applying **14,16** the temporally sequential information to the arrays of fixed memory storage units **see column 2, line 63 – column 3, line 2**; and means for successively latching and disabling **29, L1EN, L2EN, L3EN, L4EN, L5EN, L6EN** each successive fixed memory storage unit in a sequentially-connected array of said units each array becoming enabled and then un-enabled in temporal sequence , thereby directing the next temporal bit of information to the next memory storage unit in said sequentially connected array **Note: Data D0-D8 is transferred to latches 13, 17, 19, 21, 23, 25, 27 in response a respective latch enable signal L1EN, L2EN, L3EN, L4EN, L5EN, L6EN. See Fig. 6 where each latch accepts data at the rising edge of the respective latch enable signal and does not except a new data bit when a latch enable signal is logic low (disabled)**, wherein the temporally sequential information is applied along parallel inputs **see column 2, line 63 – column 3, line 2** to multiple parallel sequentially-connected-arrays of fixed memory storage units **Note: Latches 17, 19, and 21 are connected in parallel to latches 23, 25, and 27**, such that fixed memory storage unit of a given sequential order of one said array will store information originating at the same point in time, as information stored in a similar unit of the sequential order on a separate parallel array of said units **Note: Latches 23, 25, and 27 are loaded in the same sequence as latches 17, 19, and 21 (see column 8, lines 24-29**.

Pertaining to claim 7, **Fig. 1** is directed towards: A memory matrix device **11** for storing temporally sequential information **12** in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial

sequential access memory, a random access memory or a dynamic random access memory **Note: Data register 11 of Fig. 1 does not use memory addresses to address data and is neither a DRAM, serial sequential access memory, or a RAM**, comprising: sequentially-connected arrays of fixed memory storage units **17, 19, 21, 23, 25, 27**; means for applying **14,16** the temporally sequential information to the arrays of fixed memory storage units **see column 2, line 63 – column 3, line 2**; and means for successively latching and disabling **29, L1EN, L2EN, L3EN, L4EN, L5EN, L6EN** each successive fixed memory storage unit in a sequentially-connected array of said units each array becoming enabled and then un-enabled in temporal sequence , thereby directing the next temporal bit of information to the next memory storage unit in said sequentially connected array **Note: Data D0-D8 is transferred to latches 13, 17, 19, 21, 23, 25, 27 in response a respective latch enable signal L1EN, L2EN, L3EN, L4EN, L5EN, L6EN. See Fig. 6 where each latch accepts data at the rising edge of the respective latch enable signal and does not except a new data bit when a latch enable signal is logic low (disabled) Fig. 1** is directed towards: A memory matrix device **11** for storing temporally sequential information **12** in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial sequential access memory, a random access memory or a dynamic random access memory **Note: Data register 11 of Fig. 1 does not use memory addresses to address data and is neither a DRAM, serial sequential access memory, or a RAM**, comprising: sequentially-connected arrays of fixed memory storage units **17, 19, 21, 23, 25, 27**; means for applying **14,16** the temporally

sequential information to the arrays of fixed memory storage units **see column 2, line 63 – column 3, line 2**; and means for successively latching and disabling **29, L1EN, L2EN, L3EN, L4EN, L5EN, L6EN** each successive fixed memory storage unit in a sequentially-connected array of said units each array becoming enabled and then un-enabled in temporal sequence , thereby directing the next temporal bit of information to the next memory storage unit in said sequentially connected array **Note: Data D0-D8 is transferred to latches 13, 17, 19, 21, 23, 25, 27 in response a respective latch enable signal L1EN, L2EN, L3EN, L4EN, L5EN, L6EN. See Fig. 6 where each latch accepts data at the rising edge of the respective latch enable signal and does not except a new data bit when a latch enable signal is logic low (disabled)**, and further comprising: using the fixed sequentially-connected arrays as a means for subsequently reading each of the fixed memory storage units in a sequentially-connected array, or in multiple parallel sequentially-connected arrays, in the same temporal sequence in which each fixed memory storage unit was initially latched during storage, allowing retrieval of the temporal sequence of stored information without reliance on processing multiple memory addresses **Note: See column 8, lines 41-47 and Table I (EVEN RSTL=0)**.

Pertaining to claim 8, **Fig.1** is directed towards: wherein the array of fixed memory storage units includes semiconductor memory devices **Note: See Fig. 1 where latches 17, 19, 21, 23, 25, and 27 are registers used to store data of a memory**.

Pertaining to claim 13, **Fig. 1** is directed towards: a method of storing temporally sequential information **12** in an array of sequentially-connected fixed memory units**17,**

19, 21, 23, 25, 27, comprising the steps of: applying the temporally sequential information to said sequentially-connected arrays of fixed memory storage units **see column 2, line 57 – column 3, line 2**; and successively storing bits of temporally sequential information in each of the fixed memory storage units in a sequence based on the order of connection of said fixed memory storage units **see column 6, lines 63-67**, wherein the arrays of fixed memory storage units includes semiconductor memory devices and wherein **Note: See Fig. 1 where latches 17, 19, 21, 23, 25, and 27 are registers used to store data of a memory**.: the fixed memory storage units are connected in a permanent order such that whenever information is applied to the input and first fixed memory storage unit of a sequentially-connected array, the fixed memory storage units of said array are written to and latched in an invariant order **see column 6, lines 63-67**; and whenever a signal generator activates reading of the first fixed memory storage unit of the array, reading of the entire array of fixed memory storage units occurs in the same invariant order **Note: It is inherent that some circuit or "signal generator" activate the reading operation described at column 8, lines 41-47 and Table I (EVEN RSTL=0)**.

Pertaining to claim 15, **Fig. 1** is directed towards: wherein the step of applying includes the step of applying the temporally sequential information to the arrays of fixed memory storage units in parallel lines or waves **see column 2, line 57 – column 3, line 2**.

7. Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Pomet.

Pertaining to claim 12, **Figs. 3 and 7** are directed towards: A memory matrix **10** device for retrieving temporally sequential information **E**, without processing multiple memory addresses, comprising: means for activating **EN1-EN3** a pulse generator or other signal generator **MUX** to read previously-stored information in sequentially-connected arrays of fixed memory storage units **R0-R8** in the sequential order in which said fixed memory storage units are connected **(see column 5, lines 53-67)**; means for generating signals **100** transmitted through vertical arrays connecting multiple parallel sequentially-connected arrays (horizontal arrays) **(Note: Registers R0-R3 are connected in parallel to registers R4-R7, which are connected in parallel to registers R8-R11)**, to allow simultaneous signal application to temporally corresponding fixed memory storage units **see column 3, line 64 - column 4, line 3)** and consequent reading of information originating at the same point in time in different parallel horizontal arrays **see column 5, lines 53-67**; and means for successively reading the fixed memory storage units in the same sequence order in which they were latched during storage, to allow retrieval and temporal recreation of the corresponding stored temporally sequential information **see column 5, lines 53-67**.

Allowable Subject Matter

8. Claim 4 is allowed. The following is a statement of reasons for the indication of allowable subject matter. The prior art of record considered pertinent to the Applicant's disclosure, whether taken individually or in combination, does not teach or suggest: a

pulse generator whose frequency is synchronized to the frequency of input information, and the pulse generator simultaneously latching all storage units of the same sequential order in all parallel arrays through connections that are perpendicular to those of the sequentially connected arrays.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KRETELIA GRAHAM whose telephone number is (571)272-5055. The examiner can normally be reached on Mon-Fri 8am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kretelia Graham/
Examiner, Art Unit 2827

/Huan Hoang/

Primary Examiner, Art Unit 2827